APPLICANT'S REMARKS MADE IN AN AMENDMENT

Applicants have carefully reviewed and considered the Office Action mailed on January 7 2008, and the reference cited therewith.

Claims 1-8, 10-21, 23-31, and 33-65 are pending in the current application. Please charge any necessary fee or credit overpayment to Deposit Account No. 502931.

Claim Rejections Under 35 U.S.C. § 102(e)

1) The Applicable Law for Rejections under 35 U.S.C. § 102

> 35 U.S.C. 102 Conditions for patentability; novelty and loss of right to patent.
> A person shall be entitled to a patent unless –
> ...
> (e) the invention was described in - (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language;

For a cited reference to be prior art within the meaning of 35 U.S.C. § 102(e), all of the claim limitations must be anticipated by the cited reference. See MPEP 2131: "A claim is anticipated only if **each and every element** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir.1987). Additionally, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, **arranged as in the claim**." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). "The **identical invention** must be shown **in as complete detail as is contained in the ... claim.**" *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir.1989) (emphasis added).

2) Analysis

Claims 1- 8, 10-21, 23-31, & 33-65 are rejected under 35 U.S.C. 102(e) as being anticipated by Yu et al. (U.S. Patent 6,894,355), herewith referred to as "*Yu et al.*". Applicant respectfully traverses because the Office Action failed to provide the required *prima facie* case for the rejection.

The Examiner relies on *Yu et al.* for making the case for anticipation. *Yu et al.* has a priority date of January 11, 2002. The present application has the following priority dates as shown by the CROSS-REFERENCE TO RELATED APPLICATION(S) section of the present application. Specifically, paragraph [0001] of the present application states,

> "This application is a continuation-in-part of U.S. patent application Ser. No. 09/928,124, filed Aug. 10, 2001 and of U.S. patent application Ser. No. 09/928,163, filed Aug. 10, 2001. This application claims further priority to U.S. provisional patent application No. 60/381,320, filed on May 16, 2002, which is incorporated by reference in its entirety." (emphasis added)

Therefore the earliest priority date for the present application is August 10, 2001 which pre-dates *Yu et al.* Furthermore, support for each and every claim limitation of the present application is provided by U.S. patent application Ser. No. 09/928,163, filed August 10, 2001.

Paragraphs [0027]-[0029] and [0039]-[0043] of U.S. patent application Ser. No. 09/928,163 are provided below to provide assistance in showing that each and every claim limitation of the present application is supported by U.S. patent application Ser. No. 09/928,163.

> [0027] Referring to FIG. 2, semiconductor device 200 includes a substrate 210 in which a source 220 and drain 230 are formed. Substrate 210 may be composed of silicon or may be a silicon-on-insulator (SOI) substrate. Source 220 and/or drain 230 may be composed partially or fully of a rare earth silicide. Source 220 and/or drain 230 may also be composed partially or fully of platinum silicide, palladium silicide or iridium silicide. Because the source and drain are composed in part of a metal, they form Schottky contacts or Schottky-like regions 270, 275 with the substrate 210, where a "Schottky contact" is defined by the contact between a metal and a semiconductor, and a

"Schottky-like region" is a region formed by the close proximity of a semiconductor and a metal. The Schottky contacts or Schottky-like regions 270, 275 can be formed by forming the source and/or drain from a metal silicide. The Schottky contacts or Schottky-like regions 270, 275 are in an area adjacent to a channel region 240 formed between the source 220 and drain 230. The entire interface between either or both of the source 220 and the drain 230 may form a Schottky contact or Schottky-like region 270, 275 with the substrate 210. The channel region 240 may be impurity doped where the doping may be conventional non-uniform doping or may be uniform doping as described in copending U.S. patent application Ser. No. 09/465,357 and U.S. patent application Ser. No. 09/777,536.

[0028] An insulating layer 250 is formed on top of the channel region 240 and may be formed on part or all of the source 220 and drain 230. The insulating layer 250 is composed of a material with a dielectric constant greater than that of silicon dioxide; e.g. a dielectric constant greater than 3.9. For example, insulating layer 250 may be composed of a metal oxide such as TaO_2 with a dielectric constant of approximately 25, TiO_2 with a dielectric constant of approximately 50-60, HfO_2 with a dialectic constant of approximately 15-20, or ZrO_2 with a dielectric constant of approximately 15-20. The insulating layer 250 may consist of a dielectric with a modest K value (e.g., 5-10), such as nitride/oxide or oxy-nitride stack; a medium K value (e.g., 10-20), such as unary oxides Ta_2O_3, TiO_2, ZrO_2, HfO_2, Y_2O_3, La_2O_3, Gd_2O_3, Sc_2O_3 or silicates $ZrSiO_4$, $HfSiO_4$, $LaSiO_4$, or $TiSiO_4$; or a high K value (e.g., g than 20) such as amorphous $LaAlO_3$, $ZrTiO_4$, $SnTiO_4$, or $SrZrO_4$, or single crystals $LaAl_3O_4$, $BaZrO_3$, Y_2O_3, La_2O_3. Optionally, to improve manufacturability issues associated with transition metals, the insulating layer 250 may consist of more than one layer. The insulating layer 250 may be formed with a "bi-layer" approach and may consist of more than one type of dielectric, e.g., TiO_2 on top of Si_3N_4. A gate electrode 260 is positioned on

top of the insulating layer 250. A thin insulating layer 225 surrounds the gate electrode 260.

[0029] By forming a semiconductor device with (1) a source 220 or drain 230 forming a Schottky contact or Schottky-like region 270, 275 with the substrate 110; and (2) an insulating layer 250 with a relatively high dielectric constant, one is able to achieve a larger drive current I_d for larger K, but constant K/T_{ins}.

[0039] The device for regulating flow of electric current described above, for example a planar P-type or N-type MOSFET, may be formed using the process shown in FIGS. 4-8 and described in FIG. 9. (Note that the planar P-type or N-type MOSFET need not be planar in the horizontal direction, but may assume any planar orientation.) Referring to FIGS. 4 and 9, a thin screen oxide 323 is grown on silicon substrate 310, the substrate 310 having a means for electrically isolating transistors from one another (905). The thin screen oxide, optionally a thickness of 200 Å, acts as the implant mask for the channel region 340 doping. The appropriate channel dopant species (for example Arsenic and Indium for P-type and N-type devices respectively) is then ion-implanted through the screen oxide 323 to a pre-determined depth in the silicon (for example, 1000 Å) (910).

[0040] Referring to FIGS. 5 and 9, the screen oxide layer 323 of FIG. 4 is removed with hydro-fluoric acid (915), and the thin insulating layer 450 is either grown or deposited at least on a portion of the channel region 340 (920). This insulating layer 450 may consist of TiO_2, TaO_2, or any other appropriate compound with a high dielectric constant as discussed above. Immediately following the insulating layer growth or deposition, an in-situ heavily doped silicon film is deposited (930). This silicon film will eventually make up the gate electrode 460. The silicon film may be doped with phosphorus for an N-type device or boron for a P-type device. The gate

electrode 460 is then patterned with a lithographic technique and silicon etch that is highly selective to the insulating layer 450 (935).

[0041] Referring to FIGS. 6 and 9, a thin oxide, optionally approximately 100 Å in thickness, is formed on the top surface and sidewalls of the gate electrode 460 (940). Some of the oxide layers then are removed by anisotropic etch to expose the silicon on the horizontal surfaces 510, while preserving it on the vertical surfaces (945). This step serves both to create a gate sidewall oxide 525 and to electrically activate the dopants in the gate electrode 460 and channel region 340 of the device.

[0042] Referring to FIGS. 7 and 9, a metal is deposited as a blanket film, optionally approximately 400 Å thick, on all surfaces (950). The particular metal deposited will depend on whether the device is N-type or P-type. Platinum may be used for the P-type device while erbium may be used for an N-type device. The semiconductor device 600 is then annealed for a specified time at a specified temperature, for example, 45 minutes at 400C (955). Where the metal is in direct contact with the silicon, the annealing process causes a chemical reaction that converts the metal to a metal silicide 606. The metal 616 not in contact with silicon does not react.

[0043] Referring to FIGS. 8 and 9, the unreacted metal 616 is removed with a wet chemical etch (960). For example, if the deposited metal was platinum or erbium, aqua regia or HNO_3, respectively, may be used to remove it. The silicide electrodes that remain are the source 620 and drain 630. The Schottky device for regulating flow of electric current with a high dielectric constant insulating layer is now complete and ready for electrical contacting to gate electrode 460, source 620, and drain 630 (965).

Support for claims 1, 15 and 24 is located in U.S. patent application Ser. No. 09/928,163, paragraphs [0027], [0039], [0040], [0042] and [0043].

Support for claims 2, 16 and 25 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0027].

Support for claims 3, 17 and 26 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0027].

Support for claims 4, 18 and 27 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0028].

Support for claims 5, 19 and 28 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0028].

Support for claims 6, 20 and 29 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0027].

Support for claims 7, 21 and 30 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0027].

Support for claims 8, 23 and 31 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0027].

Support for claim 10 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0028].

Support for claim 11 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0028].

Support for claim 12 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0027].

Support for claim 13 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0027].

Support for claim 14 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0042].

Support for claims 33, 44 and 55 is located in U.S. patent application Ser. No. 09/928,163, paragraphs [0027], [0039], [0040], [0041], [0042] and [0043].

Support for claims 34, 45 and 56 is located in U.S. patent application Ser. No. 09/928,163, paragraphs [0040] and [0041].

Support for claims 35, 46 and 57 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0043].

Support for claims 36, 47 and 58 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0042].

Support for claims 37, 48 and 59 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0027].

Support for claims 38, 49 and 60 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0027].

Support for claims 39, 50 and 61 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0028].

Support for claims 40, 51 and 62 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0028].

Support for claims 41, 52 and 63 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0027].

Support for claims 42, 53 and 64 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0027].

Support for claims 43, 54 and 65 is located in U.S. patent application Ser. No. 09/928,163, paragraph [0042].

As each and every claim limitation of the present application is provided by U.S. patent application Ser. No. 09/928,163 with a priority date of August 10, 2001 and the present application is a continuation-in-part of U.S. patent application Ser. No. 09/928,163 and August 10, 2001 pre-dates the priority date of January 11, 2002 of *Yu et al.* the Examiner has failed to provide a *prima facie* case of anticipation for claims 1-8, 10-21, 23-31 and 33-65. Claims 1-8, 10-21, 23-31 and 33-

65 appear to be in condition for allowance and reconsideration and withdrawal of the rejection are respectfully requested.

Applicant respectfully requests reconsideration and withdrawal of the rejection. Applicant believes that the present application stands in condition for allowance.

CONCLUSION

Applicant respectfully submits that claims 1-8, 10-21, 23-31, and 33-65 are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's patent agent David King (952-223-5250) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 502931.

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CERTIFICATE OF MAILING UNDER 37 CFR 1.8: I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Washington, D.C. 22313-1450, on the 7th day of April, 2008.

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